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TRANSMITTAL FORM

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Application Number	09/832,160
Filing Date	April 9, 2001
First Named Inventor	Akram et al.
Group Art Unit	2822
Examiner Name	D. Graybill
Attorney Docket Number	2269-3846.2US (98-0796.02/US)

ENCLOSURES *(check all that apply)*

- ☒ Postcard receipt acknowledgment (attached to the front of this transmittal)
- ☒ Duplicate copy of this transmittal sheet in the event that additional filing fees are required under 37 C.F.R. § 1.16
- ☐ Preliminary Amendment
- ☐ Response to Restriction Requirement/Election of Species Requirement dated
- ☐ Amendment in response to office action dated
- ☐ Amendment under 37 C.F.R. § 1.116 in response to final office action dated
- ☐ Additional claims fee - Check No. in the amount of $
- ☐ Letter to Chief Draftsman and copy of FIGS. with changes made in red
- ☐ Transmittal of Formal Drawings
- ☐ Formal Drawings (sheets)
- ☐ Information Disclosure Statement, PTO/SB/08A (08-00); ☐ copy of cited references
- ☐ Supplemental Information Disclosure Statement; PTO/SB/08A (08-00); copy of cited references and Check No. in the amount of $180.00
- ☐ Associate Power of Attorney
- ☐ Petition for Extension of Time and Check No. in the amount of $
- ☐ Petition
- ☒ Appeal Brief (11 pages); Claims Appendix (5 pages); Check no. 8365 in the amount of $500.00
- ☐ Certified Copy of Priority Document(s)
- ☐ Assignment Papers *(for an Application)*
- ☐ Terminal Disclaimer
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- ☐ Other Enclosure(s) *(please identify below)*:

Remarks

The Commissioner is authorized to charge any additional fees required but not submitted with any document or request requiring fee payment under 37 C.F.R. §§ 1.16 and 1.17 to Deposit Account 20-1469 during pendency of this application.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm *or* Individual name	Brick G. Power — Registration No. 38,581
Signature	
Date	September 14, 2005

CERTIFICATE OF MAILING

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

Akram et al.

Serial No.: 09/832,160

Filed: April 9, 2001

For: WAFER-LEVEL PACKAGE AND METHODS OF FABRICATING

Confirmation No.: 8501

Examiner: D. Graybill

Group Art Unit: 2822

Attorney Docket No.: 2269-3846.2US

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APPEAL BRIEF

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Attn: Board of Patent Appeals and Interferences

Sir:

This APPEAL BRIEF is being submitted in the format required by 37 C.F.R. § 41.37(c)(1), with the fee required by 37 C.F.R. § 41.20(b)(2).

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I. REAL PARTY IN INTEREST

U.S. Application Serial No. 09/832,160 (hereinafter "the '160 Application"), the application at issue in the above-referenced appeal, has been assigned to Micron Technology, Inc., as evidenced by the assignment that has been recorded with the U.S. Patent & Trademark Office (hereinafter "the Office") at Reel No. 010090, Frame No. 0621. Accordingly, Micron Technology, Inc., is the real party in interest in the above-referenced appeal.

II. RELATED APPEALS AND INTERFERENCES

Neither Appellants nor their attorneys of record are aware of an appeals, interferences, or other proceedings that would affect the decision of the Board of Patent Appeals and Interferences in the above-referenced appeal.

III. STATUS OF CLAIMS

Claims 1-9 and 12-34 are currently pending in the '160 Application.

Claims 4, 9, and 23-34 have been withdrawn from consideration pursuant to an election of species requirement.

Final rejections were presented against claims 1-3, 5-8, and 12-22, which have been considered.

IV. STATUS OF AMENDMENTS

The '160 Application was filed with thirty-four (34) claims on April 9, 2001.

A Preliminary Amendment was filed on July 9, 2001.

On December 21, 2001, a first action on the merits of claims 1-34 was mailed. In that action, each of claims 1-34 stood rejected under the doctrine of obviousness-type double patenting. A response to the first Office Action, including a terminal disclaimer and the appropriate fee, was mailed on February 7, 2002.

As no further action had been taken by the examiner by September 6, 2002, a Status Inquiry was filed.

After nearly a year, on January 14, 2003, an Election of Species Requirement was made. A Response to the Election of Species Requirement was promptly filed on January 28, 2003. Several months later, on May 20, 2003, a Notice of Non-Compliant Response was mailed. In an attempt to correct what the Examiner perceived to be deficiencies in the Response, another Response was mailed on June 5, 2005. That Response was followed by another Notice of Non-Compliant Response, which was mailed by the Office on August 22, 2003, in which the Examiner clarified the elections that were to be made in response to a convoluted set of election of species and restriction requirements. Another response was mailed on September 5, 2003.

Finally, on December 18, 2003, a second, non-final Office Action was mailed. In that action, the Examiner indicated that claims 4, 9, and 23-34 had been withdrawn from consideration. New grounds of rejection were presented against claims 1-3, 5-8, and 10-22. In response to the rejections presented in the Office Action of December 18, 2003, an Amendment was filed on March 18, 2004. Claims 10 and 11 were canceled without prejudice or disclaimer in that Amendment.

Despite the amendments and detailed explanations as to the patentability of the claims that had been rejected, the Examiner maintained all of his rejections in a Final Office Action,

which was mailed on May 28, 2004. Appellants responded by filing an Amendment Under 37 C.F.R. § 1.116 on July 28, 2004, in which a minor revision to claim 1 was presented. The Examiner refused to enter the amendment and only "cursorily considered" the accompanying remarks, as evidenced by the Advisory Action dated August 26, 2004.

A Request for Continued Examination (RCE) was filed on August 30, 2004.

On November 12, 2004, another non-final action was mailed. The same rejections were maintained. An Amendment, which was filed on February 14, 2005, included further remarks as to the patentability of the claims that had been considered.

The Examiner has continued to disregard the simple, point-by-point explanations of the differences between the subject matter disclosed in the cited art and that recited in the claims, as evidenced by the Final Office Action of April 25, 2005. Despite the submission of another explanatory Response to Final Office Action, which was mailed on June 27, 2005, the Examiner continues to maintain his rejections, with mere cursory consideration by the Examiner, as indicated in the Advisory Action dated July 8, 2005.

In view of the Examiner's continued rejection of the claims, a Notice of Appeal was filed on July 14, 2005.

This APPEAL BRIEF follows the Notice of Appeal, and is being submitted within two months of the mailing date of the Notice of Appeal.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The claims of the above-referenced application are directed to methods for fabricating chip-scale packages. Such a method includes disposing a polymeric film over a semiconductor

device. *See, e.g.,* paragraph **[0014]**. The film may be preformed or formed from an unconsolidated quantity of photoimageable material that has been disposed on a surface of the semiconductor device. *See, e.g., id.* At least one aperture that extends through the film is aligned with a corresponding bond pad of the semiconductor device. *See, e.g.,* paragraph **[0015]**. Conductive material is selectively introduced into the at least one aperture. *See, e.g.,* paragraph **[0016]**. Such selective introduction may include bondinf othe conductive mateiral to the corresponding bond pad. *See, e.g., id.*

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(A) Claims 1-3, 5-8, and 12-20 stand rejected under 35 U.S.C. § 102(b) for reciting subject matter which is purportedly anticipated by the disclosure of U.S. Patent 6,255,737 to Hashimoto (hereinafter "Hashimoto"); and

(B) Claims 21 and 22 have been rejected under 35 U.S.C. § 103(a) for being drawn to subject matter which is purportedly unpatentable over the teachings of Hashimoto, in view of teachings from U.S. Patent 6,294,407 to Jacobs (hereinafter "Jacobs").

VII. ARGUMENT

A. REJECTIONS UNDER 35 U.S.C. § 102

1. APPLICABLE LAW

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference which qualifies as prior art under 35 U.S.C. § 102. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053

(Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

2. REFERENCE RELIED UPON

Hashimoto

The description of Hashimoto is directed to, among other things, a process that includes applying a preformed sheet of polyimide 64 to a wafer 60 carrying a plurality of semiconductor devices. FIGs. 13A and 13B; col. 11, lines 45-48. Apertures 64a are formed through the preformed sheet 64 following application thereof to the wafer 60 to expose bond pads 62 of the semiconductor devices through the preformed polyimide layer 64. FIG. 13C; col. 11, lines 49-52. Conductive material 68 may then be introduced into the apertures 64a and into contact with the bond pads 62. FIG. 13D; col. 11, lines 49-54. As noted in the Final Office Action, Hashimoto also indicates that apertures may be formed through a stress relieving layer by "predrilling." Col. 11, lines 63-66.

Hashimoto also notes, at col. 4, line 66, to col. 5, line 20, that *every* bond pad (electrode 12) of a semiconductor chip 1 is rerouted by wires 3 to an external electrode 5 that is more centrally located over an active surface 1a of the semiconductor chip 1. The wires 3 and redirected external electrodes 5 are at least partially formed by non-selectively sputtering a layer of aluminum or other conductive material (*e.g.*, conductive material 68) over the entire surface of a stress relieving layer 7 (*e.g.*, preformed sheet of polyimide 64), then patterning the layer of conductive material.

3. ANALYSIS

Independent claim 1 recites a method for fabricating a chip-scale package. The method of independent claim 1 includes positioning a preformed polymeric film over a semiconductor device. The preformed polymeric film includes at least one aperture that extends substantially longitudinally therethrough. When the preformed polymeric film is positioned over the at least one semiconductor device, the at least one aperture is in substantial alignment with a corresponding bond pad of the semiconductor device. The method of independent claim 1 also includes selectively introducing conductive material into the at least one aperture.

As those of ordinary skill in the art would readily understand from the disclosure of the above-referenced application, "selectively introducing" refers to the process by which the conductive material is introduced (*e.g.,* selective deposition vs. blanket deposition), not to the time ("when") or the location at which ("where") (such as at a particular facility, in a particular deposition chamber, etc.) the conductive material is introduced, as has been asserted by the Examiner. Final Office Action, page 4.

The specification of the above-referenced application, at paragraphs **[0062]** and **[0083]**, provides nonlimiting examples of selective introduction of conductive material into the apertures of a polymeric film. From these examples, one of ordinary skill in the art would readily understand that "selectively introducing" conductive material results in a structure that includes conductive material within the apertures of a polymeric film, but substantially no conductive material on an exposed surface of the polymeric film, as would occur during blanket deposition processes of the type described in Hashimoto.

Moreover, one of ordinary skill in the art would readily understand the meaning of the term "selective" when used in conjunction with processes for depositing or otherwise forming material layers. This fact is evidenced by the discussions at pages 155-156 of Wolf et al., Silicon Processing for the VLSI Era, Volume 1 – Process Technology (Lattice Press, 1986) (hereinafter "Wolf") and U.S. Patent 6,245,674 to Sandhu et al. (hereinafter "Sandhu"), copies of which were provided to the Examiner during prosecution of the above-referenced application.

In contrast to independent claim 1, Hashimoto lacks any express or inherent description of *selectively* introducing conductive material into the apertures of a preformed polymeric film.

Rather than disclosing selective introduction, the express description of Hashimoto is limited to blanket deposition of conductive films over the stress relieving layers described therein to introduce conductive material into the apertures of such stress relieving layers and, thus, into contact with the bond pads (*e.g.,* electrodes 12) of a semiconductor device (*e.g.,* semiconductor chip 1). The result of such blanket deposition is that conductive material is not located only within the apertures of the stress relieving layer, but also covers the surfaces of the stress relieving layers, and must subsequently be removed therefrom to prevent electrical shorting between the bond pads of the semiconductor device.

Further, as Hashimoto discloses the suitability of blanket deposition processes for introducing conductive material 68 into the apertures 64a of a preformed polyimide plate 64, it is clearly not necessary, or inherent, that conductive material 68 be introduces into the apertures 64a in a selective manner.

Therefore, Hashimoto does not anticipate each and every element of independent claim 1, as would be required to maintain the 35 U.S.C. § 102(e) rejection of independent claim 1.

Each of claims 2, 3, 5-8, and 12-20 is allowable, among other reasons, for depending either directly or indirectly from claim 1, which is allowable.

Claim 19 is further allowable since Hashimoto does not expressly or inherently describe placing a preformed polymeric film on at least a portion of a peripheral edge of a semiconductor device. While Hashimoto does note that a polyimide plate 64 may be "adhered to a wafer 60" (col. 11, lines 45-47), Hashimoto does not mention that the polyimide plate 64 extends onto peripheral edges of the wafer or any of the semiconductor devices carried thereby or that such extension of the polyimide plate 64 onto the peripheral edges is necessary, or inherent.

Claim 20 is additionally allowable since Hashimoto lacks any express or inherent description of placing polymeric material at least laterally adjacent a conductive structure. Instead, the description of Hashimoto is limited to forming "outermost layer[s] (protective layer[s])," which partially surround conductive structures. Col. 12, lines 50-52 and 62-64.

In view of the foregoing, reversal of the 35 U.S.C. § 102(b) rejections of claims 1-3, 5-8, and 12-20 is respectfully solicited.

B. REJECTIONS UNDER 35 U.S.C. § 103(a)

Claims 21 and 22 stand rejected under 35 U.S.C. § 103(a) for being drawn to subject matter which is purportedly unpatentable over the teachings of Hashimoto, in view of teachings from Jacobs.

Claims 21 and 22 are both allowable, among other reasons, for depending indirectly from claim 1, which is allowable.

Accordingly, reversal of the 35 U.S.C. § 103(a) rejections of claims 21 and 22 is respectfully requested.

C. ELECTION OF SPECIES REQUIREMENT

It is respectfully submitted that independent claim 1 remains generic to all of the species of invention of the second group that was identified in the Election of Species Requirement in the above-referenced application. In view of the allowability of these claims, claims 4, 9, and 23-34, which have been withdrawn from consideration, should also be considered and allowed. M.P.E.P. § 806.04(d).

VIII. CLAIMS APPENDIX

The current status of each claim that has been introduced into the above-referenced application is set forth in CLAIMS APPENDIX to this Appeal Brief.

IX. EVIDENCE APPENDIX

No evidence has been submitted pursuant to 37 C.F.R. §§ 1.130, 1.131, or 1.132. Accordingly, no evidence appendix accompanies this Appeal Brief.

X. RELATED PROCEEDINGS APPENDIX

No decisions have been rendered by the Board or any court in a related application. Therefore, this Appeal Brief is not accompanied by a related proceedings appendix.

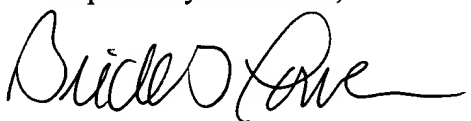
XI. CONCLUSION

(A) Claims 1-3, 5-8, and 12-20 are allowable under 35 U.S.C. § 102(b) for reciting subject matter which is not anticipated by the disclosure of Hashimoto; and

(B) Claims 21 and 22 are allowable under 35 U.S.C. § 103(a) for being drawn to subject matter which is not obvious over teachings from Hashimoto and Jacobs.

Therefore, the rejections of claims 1-3, 5-8, and 12-22 should be reversed. Additionally, claims 4, 9, and 23-34 should be returned to consideration, and each of claims 1-9 and 12-34 should be allowed.

Respectfully submitted,



Brick G. Power
Registration No. 38,581
Attorney for Applicants
TRASKBRITT, PC
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: September 14, 2005
BGP/eg
Document in ProLaw

CLAIMS APPENDIX

1. A method for fabricating a chip-scale package, comprising:

positioning a preformed polymeric film including at least one aperture that extends substantially longitudinally therethrough over a semiconductor device with the at least one aperture in substantial alignment with a corresponding bond pad of the semiconductor device; and

selectively introducing conductive material into the at least one aperture.

2. The method of claim 1, further comprising adhering the preformed polymeric film to the semiconductor device.

3. The method of claim 1, further comprising defining at least another aperture through the preformed polymeric film.

4. The method of claim 3, wherein defining is effected after positioning.

5. The method of claim 3, wherein defining is effected before positioning.

6. The method of claim 1, wherein introducing comprises bonding the conductive material to the corresponding bond pad.

7. The method of claim 1, wherein introducing comprises depositing the conductive material onto the preformed polymeric film and within the at least one aperture.

8. The method of claim 7, wherein depositing comprises chemical vapor depositing or physical vapor depositing the conductive material.

9. The method of claim 1, wherein introducing comprises placing a preformed conductive structure within the at least one aperture.

12. The method of claim 1, further comprising forming at least one contact at an end of the conductive material, opposite the semiconductor device.

13. The method of claim 12, further comprising placing a conductive structure adjacent the at least one contact.

14. The method of claim 13, wherein placing comprises applying solder to the at least one contact.

15. The method of claim 1, further comprising positioning at least one conductive trace on the preformed polymeric film and in communication with the conductive material.

16. The method of claim 15, further comprising forming at least one contact in communication with the conductive trace.

17. The method of claim 16, further comprising placing a conductive structure adjacent the at least one contact.

18. The method of claim 17, wherein placing comprises applying solder to the at least one contact.

19. The method of claim 1, further comprising placing the preformed polymeric film on at least a portion of a peripheral edge of the semiconductor device.

20. The method of claim 17, further comprising placing polymeric material at least laterally adjacent the conductive structure.

21. The method of claim 17, further comprising placing a conductive elastomer over at least one conductive structure.

22. The method of claim 21, further comprising placing another conductive structure in contact with the conductive elastomer, opposite the at least one conductive structure.

23. A method for fabricating a chip-scale package, comprising:

placing photoimageable polymeric material on a surface of a semiconductor device;

forming a polymeric film from the photoimageable polymeric material with at least one aperture extending substantially longitudinally through the polymeric film, the at least one aperture aligned with a corresponding bond pad of the semiconductor device; and introducing conductive material into the at least one aperture.

24. The method of claim 23, wherein forming comprises selectively exposing regions of the photoimageable polymeric material to electromagnetic radiation.

25. The method of claim 23, further comprising defining the at least one aperture through the polymeric film.

26. The method of claim 25, wherein defining is effected after the forming.

27. The method of claim 25, wherein defining is effected substantially simultaneously with the forming.

28. The method of claim 23, further comprising placing at least one conductive trace on the polymeric film and in communication with the conductive material.

29. The method of claim 28, further comprising placing at least one contact in communication with the at least one conductive trace.

30. The method of claim 29, further comprising placing at least one conductive structure adjacent the at least one contact.

31. The method of claim 30, further comprising placing polymeric material at least laterally adjacent the at least one conductive structure.

32. The method of claim 30, further comprising placing a conductive elastomer over the at least one conductive structure.

33. The method of claim 32, further comprising placing at least one other conductive structure in contact with the conductive elastomer, opposite the at least one conductive structure.

34. The method of claim 23, wherein forming comprises forming the polymeric film so as to extend at least partially over a peripheral edge of the semiconductor device.